CY15FRAMKIT-002 Serial F-RAM Development Kit

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Drawing Numbers

PCBA	121-60533-01
PCB	600-60533-01
FAB DRW	610-60533-01
ASSY DRW	620-60533-01
SCH DRW	630-60533-01

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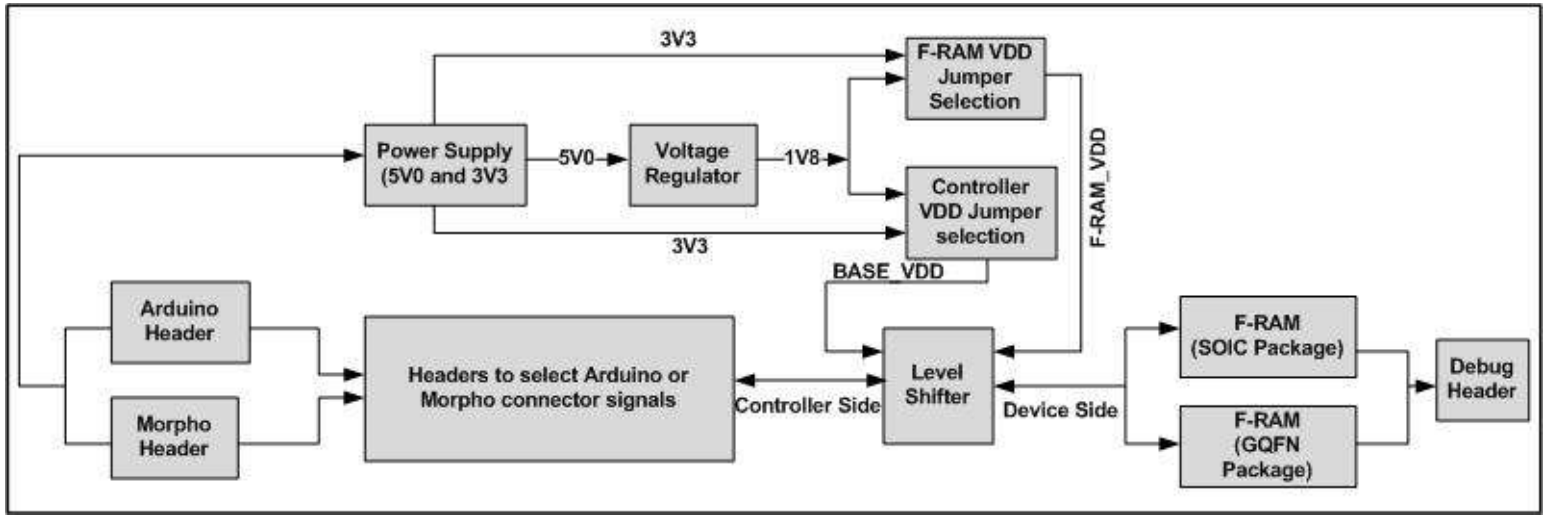
CY15FRAMKIT-002 Block Diagram



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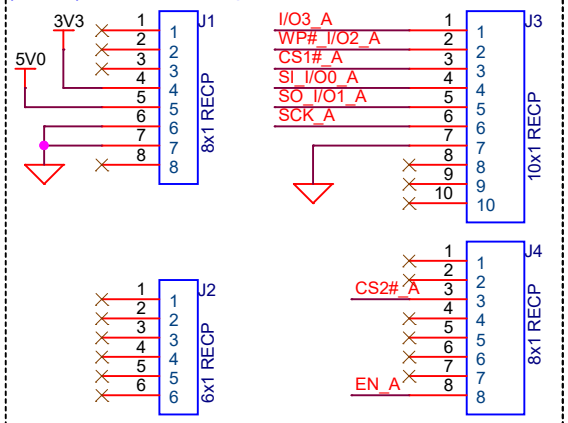
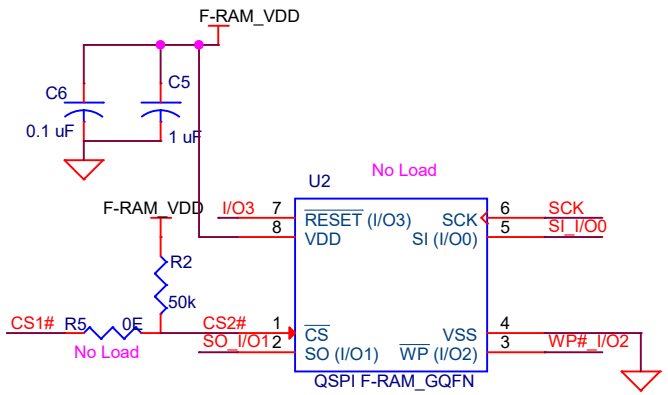
(J1-J4) Arduino Compatible male Headers

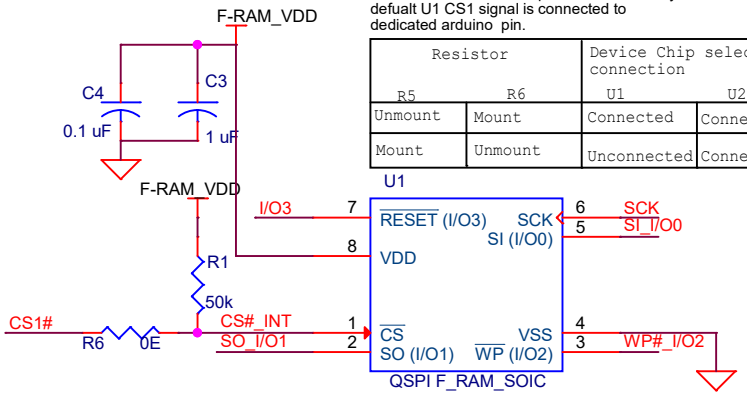


QSPI F-RAM

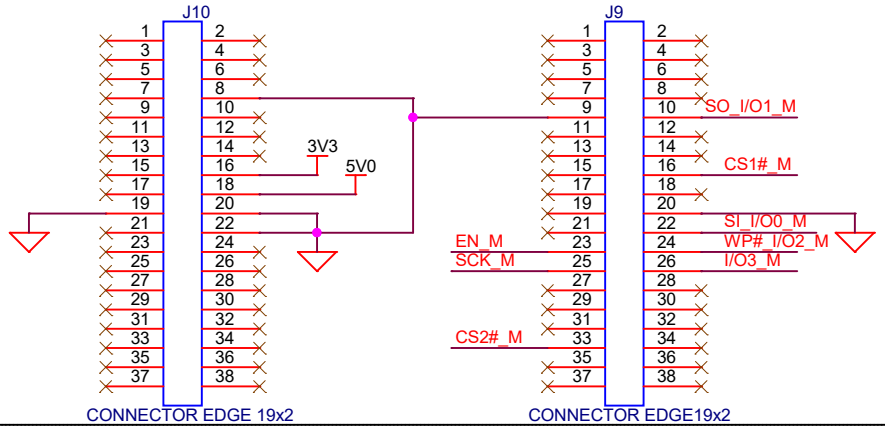


Solder R5 and remove R6 to connect CS2 of U2 to dedicated arduino pin which is CS1. By defualt U1 CS1 signal is connected to dedicated arduino pin.

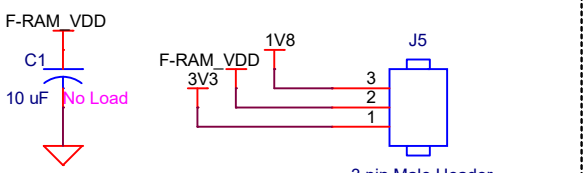
Resistor		Device Chip select connection	
R5	R6	U1	U2
Unmount	Mount	Connected	Connected
Mount	Unmount	Unconnected	Connected



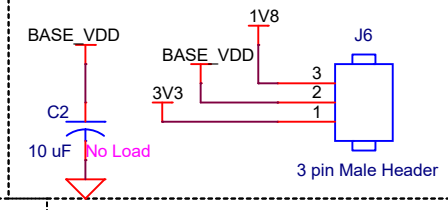
(J9-J10) Morpho Compatible female Headers



F-RAM VDD selection

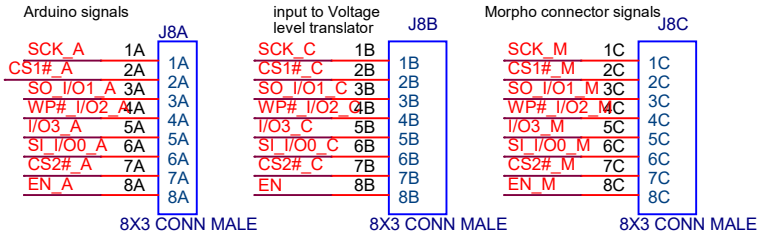


Controller VDD selection

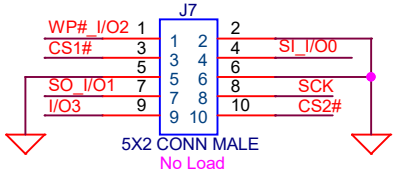


connect aurdino I/Os to device by shorting J8A and J8B through jumper.

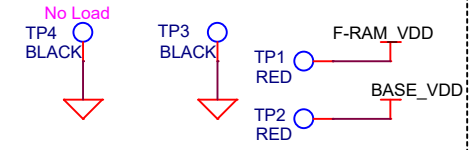
connect Morpho I/Os to device by shorting J8C and J8B through jumper.



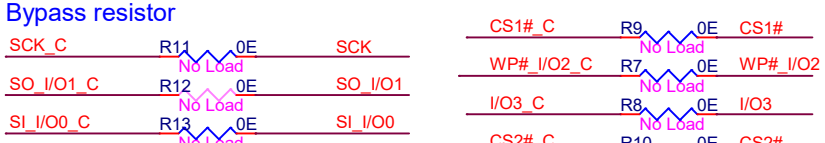
Debug Header



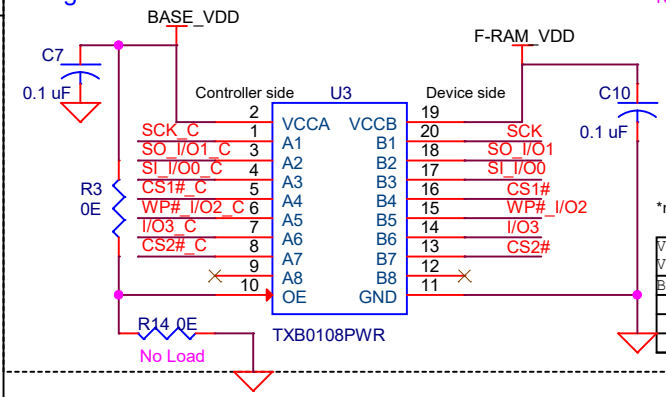
Test points



Bypass resistor



Voltage Level Translator

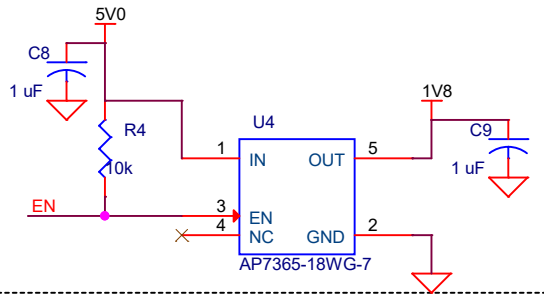


Mount R14 to bypass voltage Translator and mount R7 to R13 to connect signals from Arduino/Morpho connector to F-RAM device.

*make sure that VCCA<=VCCB

Valid Power Selection for Voltage Level Translator	
BASE_VDD (J6)	F-RAM_VDD (J5)
1V8	1V8
1V8	3V3
3V3	3V3

1.8V Regulator



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REVISION HISTORY

REV	DESCRIPTION OF CHANGE	DATE
01	Internal Release	2018/01/22
02	Initial Release Updated volatge regulator part (AP7365-18WG-7) Changed J5 and J6 from 6 pin to 3 pin connector Updated Schematic Template	2018/08/27

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